5116S/L
2K x 8-BIT CMOS STATIC RAM

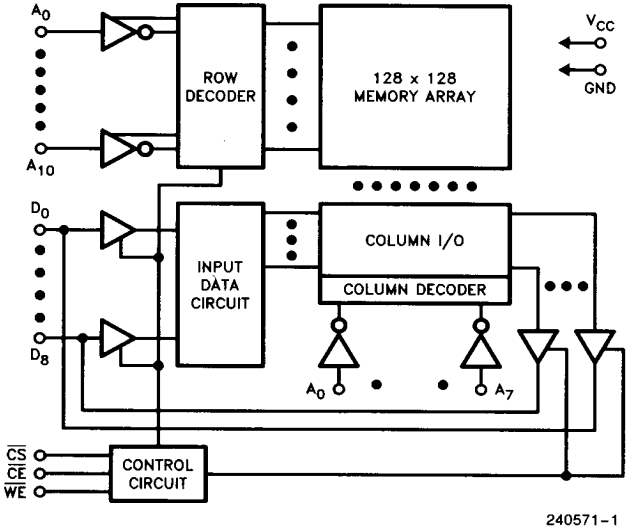
	5116S-10	5116S-12	Unit
Address Access Time (t_{AA})	100	120	ns
Chip Select Access Time (t_{ACS})	100	120	ns
Output Enable Access Time (t_{OE})	40	50	ns

- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **High Reliability 24-Pin 600 Mil PDIP Package**

The 5116S is a 2048-word by 8-bit CMOS static RAM fabricated using CMOS Silicon Gate process.

When the Chip Select is brought high, the device assumes a standby mode in which the standby current is reduced to 2 μA (max). The 5116S has a data retention mode that guarantees that data will remain at minimum power supply voltage of 2.0V.

Block Diagram



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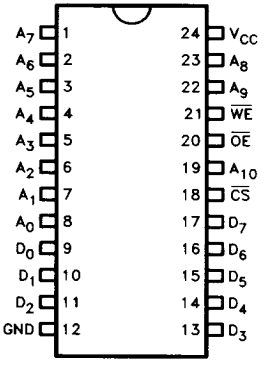
Pin Connections



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Pin Names

A_0–A_{10}	Address Input
D_0–D_7	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power
GND	Ground

October 1989
Order Number: 240571-002

Device Operation

The 5116S has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin and should be used for device operation. $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins.

Standby Power

The 5116S is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Standby	High Z	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	X	H	Read	High Z	Active

Write Mode

Write Cycles may be controlled by either $\overline{WE}$ or $\overline{CS}$. In either case, both $\overline{WE}$ and $\overline{CS}$ must be high (V_{IH}) during address transitions. During a $\overline{WE}$ Controlled write cycle, $\overline{CS}$ must be held low (V_{IL}) while $\overline{WE}$ is low. Address transfers occur on the falling edge of $\overline{WE}$ and the data transfers on rising edge of $\overline{WE}$. During a $\overline{CS}$ controlled cycle, $\overline{WE}$ must be held low (V_{IL}) while $\overline{CS}$ is low. The addresses are then transferred on the falling edge of $\overline{CS}$ and data on the rising edge of $\overline{CS}$. Data, in both cases, must be valid for a time t_{DW} before the controlling input is brought high (V_{IH}) and remain valid for a time t_{DH} after the controlling input is high.

Read Mode

$\overline{CS}$ must be low (V_{IL}) and $\overline{WE}$ must be high (V_{IH}) to activate a read cycle and obtain data at the outputs. Given stable addresses, valid data is available after a time t_{AA}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_{IN}, V_{OUT}) ..... −0.3V to +7V
Storage Temperature (T_{stg}) ..... −55°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −3.5V for periods less than 20 ns.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		6	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		8	pF

NOTE:
This parameter is sampled and not 100% tested.

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D.C. AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

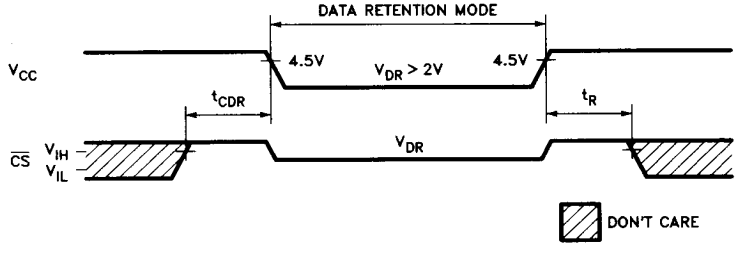
Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
I_{CC1}	Operating Current			30	40	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs open
I_{CC2}	Dynamic Current			30	60	mA	T_{cyc} = Min, V_{CC} = Max Outputs open
I_{SB}	Standby Current				3	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		STD		4	50	μA	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} = GND to V_{CC}
		L		0.2*	2		
I_{LI}	Input Load Current		−1		1	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage		−1		1	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = GND to V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −1.0 mA
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2.1 mA

*T_A = 25°C

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CDR}	Voltage for Data Retention		2			V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≥ V_{CC} − 0.2V		0.05	2	μA
t_{CDR}	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Low V_{CC} Data Retention Waveform



A.C. TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times ..... 10 ns
Timing Reference Level 1.5V
Output Load ..... 1 TTL Load + 100 pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

READ CYCLE

Symbol	Parameter	5116S-10		5116S-12		Unit
		Min	Max	Min	Max	
t_{RC}	READ Cycle Time	100		120		ns
t_{AA}	Address Access Time		100		120	ns
t_{ACS}	Chip Select Access Time		100		120	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{CLZ}	Chip Selection to Output in Low Z	10		10		ns
t_{CHZ}	Chip Deselection to Output in High Z	0	40	0	40	ns
t_{OE}	Output Enable Access Time	40		50		ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		ns
t_{OHZ}	Output Enable to Output in High Z	0	40	0	40	ns

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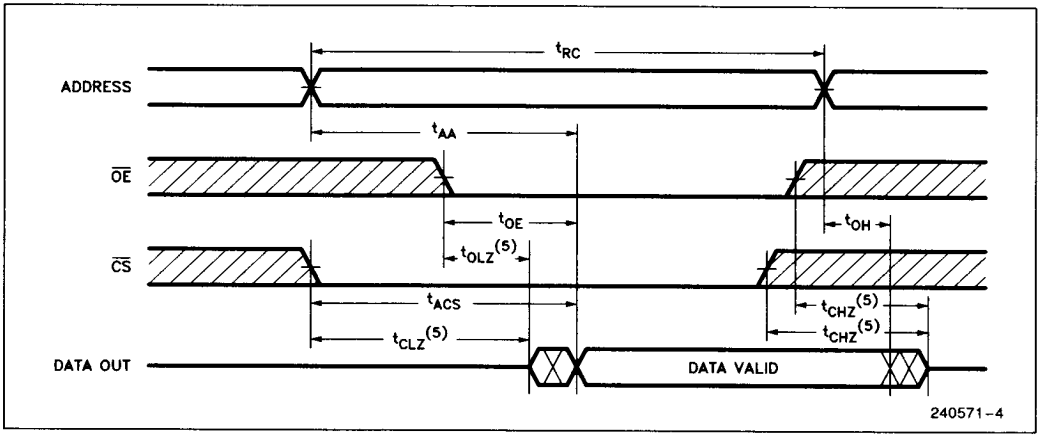
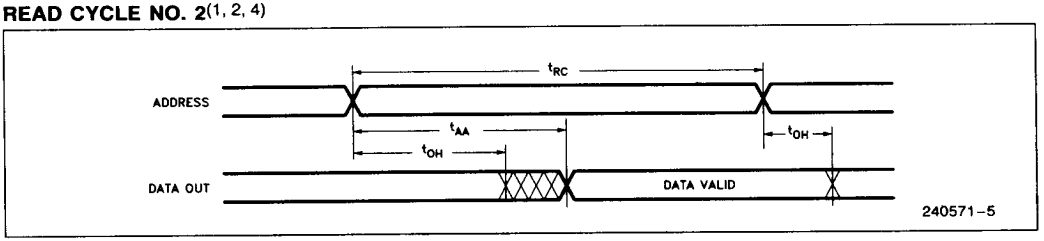
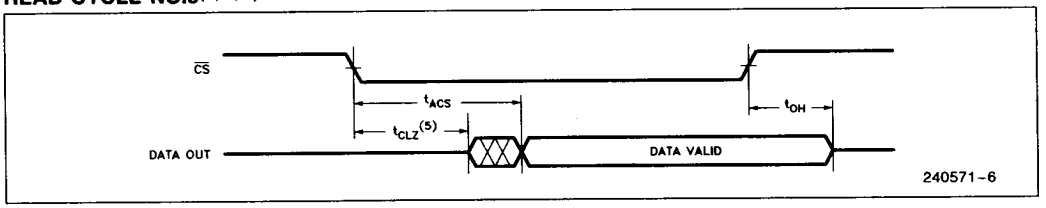
READ CYCLE NO. 1(1)



READ CYCLE NO. 2(1, 2, 4)



READ CYCLE NO.3(1, 3, 4)



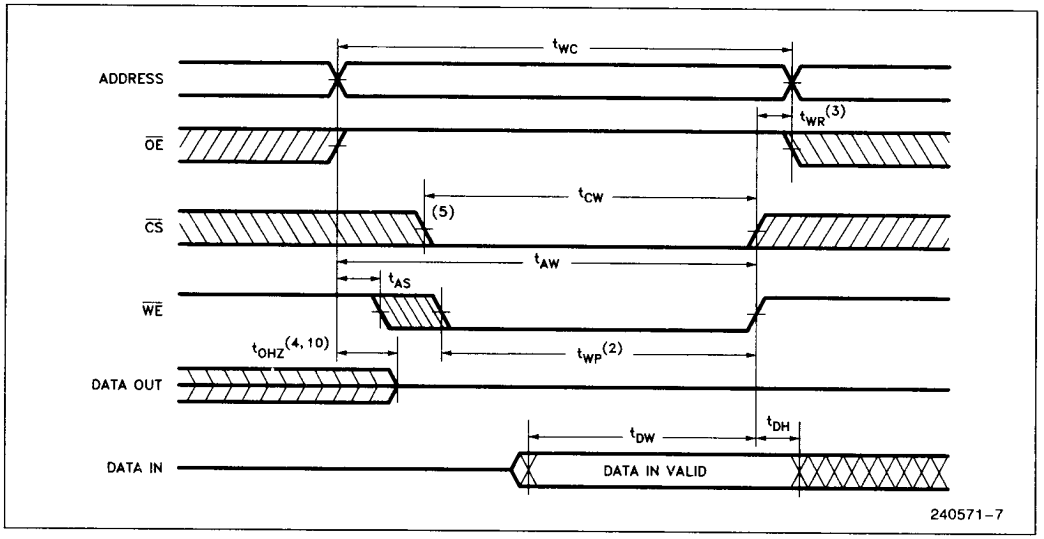
NOTES:
1. $\overline{WE}$ is high for READ Cycle. The first transitioning address.
2. Device is continuously selected; $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured at ±500 mV from steady state voltage.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10% (Continued)

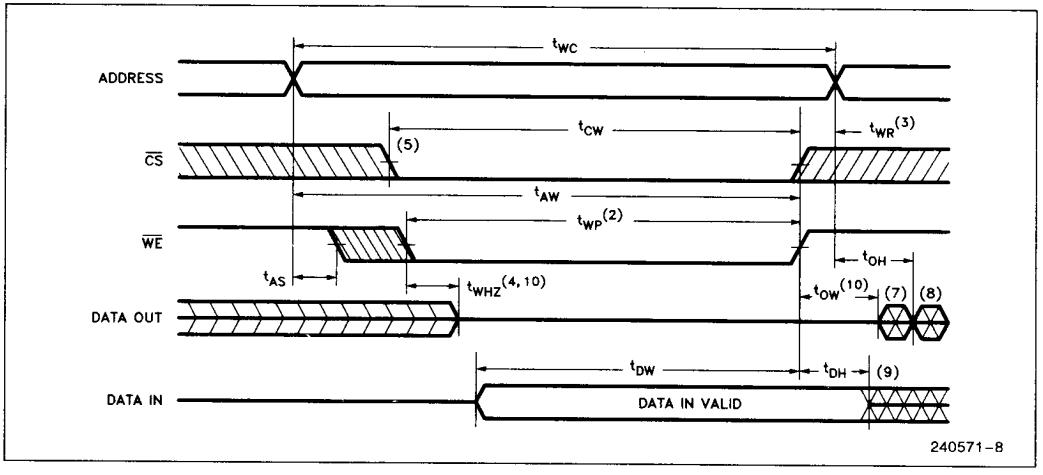
WRITE CYCLE

Symbol	Parameter	5116S-10		5116S-12		Unit
		Min	Max	Min	Max	
t_{WC}	WRITE Cycle Time	100		120		ns
t_{CW}	Chip Selection to End of Write	65		70		ns
t_{AW}	Address Valid to End of Write	80		105		ns
t_{AS}	Address Set-Up Time	0		0		ns
t_{WP}	Write Pulse Width	60		70		ns
t_{WR}	Write Recovery Time	10		10		ns
t_{DW}	Data Valid to End of Write	30		35		ns
t_{DH}	Data Hold Time	10		10		ns
t_{WHZ}	Write Enable to Output in High Z	0	30	0	35	ns
t_{OW}	Output Active from End of Write	10		10		ns
t_{OHZ}	Output Disable to Output in High Z	0	40	0	40	ns

WRITE CYCLE NO. 1(1)



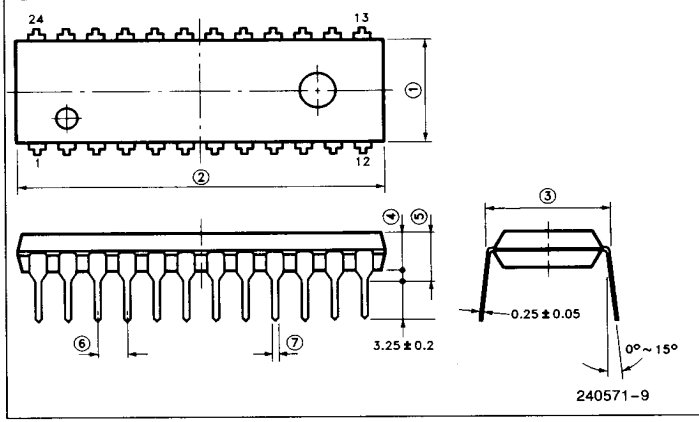
WRITE CYCLE NO. 2(1, 6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
4. During this period, I/O pins are in tri-state.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in tri-state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data on this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in output state.
10. Transition is measured at ±500 mV from steady state voltage.

PACKAGE OUTLINE

24-DIP



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	Normal	Shrink
①	13.2±0.25	6.35±0.2
②	31.0±0.3	22.0±0.25
③	15.24TYP.	7.62TYP.
④	4.25±0.2	3.45±0.2
⑤	5.1±0.2	4.2±0.2
⑥	P−2.54TYP.	P−1.778TYP.
⑦	0.5±0.1	0.46±0.1